Se	arcti ivo	nes
		ORITO IROU BIRLEDA

Application/Control No.	Applicant(s)/Patent under Reexamination
10/649,625	SEKI, YUICHI
Examiner	Art Unit
Jim Vannucci	2828

	SEAR	CHED	
Class	Subclass	Date	Examiner

INT	INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner	

SEARCH NOTES (INCLUDING SEARCH STRATEGY)			
	DATE	EXMR	
wafer lot, laser chips	11/8/2005	JV	